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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,863	01/22/2004	Eino Jacobs	PHA 23122B	5930

24737 7590 01/22/2007
PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
PAN, DANIEL H	
ART UNIT	PAPER NUMBER
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/762,863	JACOBS ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/22/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-20 are presented for examination. However, applicant is also advised to clarify the claim status of the paper filed on 01/22/04 in the next response. For examination purpose, claims 1-20 are examined based on the most recent filed claims on 05/24/04 and the applicant's elected Group I on 11/06/06.

2. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: The omitted elements are the interface connections of the distinct functional units of the VLIW processor that commencing the execution in the same cycle.

3. As to claim 18, the language "explanation of notation" and "means" are unclear. Clarification is suggested.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claim 1 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 4 of U.S. Patent No. 5,878,267. Although the conflicting claims are not identical, they are not patentably distinct from each other because although patented claim 4 did not specifically recites the chosen finite length is being dependent upon at least one feature of the operation as recited in the current claim 1, it would have been obvious to one of ordinary skill in the art to use finite length dependent on the feature of the operation as claimed because the patented claim also taught each operation having an executable form having respective executable operation length (see patented claim 4, lines 16-19), which was recognizable by one of ordinary skill in the art that specific length of was also dependent on corresponding operation feature (e.g. the executable operation).

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

5. Claims 1,3-12,14, 18, 19, 20 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1, 3-12,15, 16, 17, 20, respectively, of prior U.S. Patent No. 5,826,054. This is a double patenting rejection.

6. As to claims 1,3-12,14, 18, 19, 20, current claims 1,3-12,14, 18, 19, 20 are the same as the patented claims 1, 3-12,15, 16, 17, 20, respectively . Applicant is advised to clarify the issue.

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. Claims 1-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The reason are given below.

8. As to claim 1, no substantial practical application can be found in the claim. The practical application of the VLIW instruction and the compressed non-null operations is not clear. Although claim 1 recites the assigns a compress operation length to the operation and being chosen from the plurality of finite length. However, this is an intended use, not a final result. Applicant is reminded that the focus is not on the feature of step taken to achieved a final result which is useful, tangible, and concrete, but rather a final result achieved witch is which is useful, tangible, and concrete (see MPEP 2100-12-17). Although applicant additionally recites a computer medium comprising a stored VLIW instruction, no specific instruction component which imparts the functionalities of

the computer has been recited in the claim. Therefore, no substantial practical application can be found.

9. As to claim 2, clam 2 is directed to operation lengths. Lengths are abstract idea. As to claim 3, claim 3 is directed to a feature. No substantial practical application can be found in the claim.

10. As to claim 4, claim 4 is directed to a table. No substantial practical application can be found in the claim. Furthermore, the table includes aliased operation types. Operation types are not functional descriptive material.

11. As to claim 5, claim is directed to number. Number id abstract idea.

12. As to claim 7, no final result can be found for specifying the register file address specified by the sub-field.

13. As to claim 8, the practical application of the instruction formats is not clear.

14. As to claims 9,10, specifying issue slots of the processor to be used by some instruction is an intended result.

15. As to claims 11-15, number of bytes and lengths are abstract idea.

16. As to claim 16, practical application of aligning with the byte boundary is unclear.

17. As to claim 17, practical application of specifying the issue slots is not clear.

18. As to claims 18,19, the formatted and the encoded features in claim 18 are intended use, no practical application ahs been achieved.

19. As to claim 20, the take is non-functional descriptive material.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moreno (5,669,001) in view of Yoshida (5,761,470).

21. As to claim 1, Moreno taught at least :

a) a computer storage medium (see the cache storage in fig.4ab) comprising a stored VLIW instruction, the instruction comprised a plurality of operations and executing in parallel (see parallel execution in col.4, lines 34, col.6, lines 49-54) on distinct functional units of a VLIW processor (see the resources required for execution and the number of functional units in col.4, lines 60-65, col.8, lines 14-26, see also multiple functional units in col.1, lines 15-25 for background), each non-null operation being compressed according to a compression scheme which assigns a compressed operation length (see variable length in col.3, lines 35-44 and fixed length in col.3, lines 45-51) and the length being chosen from a plurality of finite lengths (see variable lengths), which finite lengths include at least two non-zero lengths (see any two lengths in the cache in fig.4)

and being dependent upon at least one feature of the operation (see the operation code in each VLIW).

22. Moreno did not specifically sow executing the VLIW instructions in a same machine cycle as claimed. However, Yoshida taught execution of VLIW instructions in a same cycle (see the execution of the remaining operations in col.15, lines 35-36, 40-41)). It would have been obvious to one of ordinary skill in the e art to use Yoshida in Moreno for executing VLIW instructions in a same cycle as claimed because the use of Yoshida cold provide Moreno the ability to perform the processing of VLIW instructions within a predetermined period, and therefore\, minimize the likely latency due to the instructing hazards, and because Moreno also taught the execution of his VLIW instruction in parallel to achieve the efficiency of the processing (see parallel execution in col.4, lines 34, col.6, lines 49-54), which was an indication of the desirability to execute the VLIW instructions in a same cycle, and for doing so, provided a motivation.

23. As to claim 2, since Moreno was directed variable length (see col.3, lines 35-38), and since short VLIWs were also expanded to match the resource size (col.3, lines 45-51), It must have encompassed any length, such as in the range of 0 to any longer length.

24. As to claim 3, Moreno also taught an abbreviated opcode (see op1,op5, etc. in col.6, lines 1-23), guarded or unguarded (see target address at branch AB in col.3, lines 5-10), resultless (see col.6, line 5 c3), immediate parameter with fixed bits (see primitive operation of a word length in col.4, line 60-62).

25. As to claim 6, see the branch in the tree instructions in main memory in col.3, lines 30-35.

26. As to claim 15, see variable length in col.3, lines 35-44 and col.9, lines 25-32.

27. As to claim 16, see the aligned positions of base 32 bytes in col.9, lines 36-45.

28. As to claim 4, Moreno did not specifically show the operation types are aliases according ton the table as claimed. However, since no specific operation ahs been reflected into the claim, the aliased operation types are read as any operations type in general . Yoshida taught operat0n types were aliased as a table (see fig.2, the aliased operation of 2-ops and 3-ops). It would have been obvious to one of ordinary skill in the art to include aliased operation types in table as claimed because the use of Yoshida could provide Moreno the ability to map his operations a predetermined set of types of a given format, and it could be readily achieved by reconfiguring the operation types of Yoshida into Moreno with modified control parameters (e.g. table R/W ports) so that the aliased operation types of Yoshida could be recognized by Moreno, and because Moreno also taught the compatibility in a processor allowing that same program to be executed in scalar, superscalar and VLIW implementation (see col.2, lines 52-59), which was a suggestion of the need for creating a map, such as an aliased table, to the operation types of the architecture in order to enhance the adaptability of the system , and in doing so, provided motivation.

29. As to claim 5, see a word length in col.4, line 60-62.

30. As to claim 7, Moreno did specifically show the subfield specifying register file addresses as claimed. However Yoshida taught subfield specifying the register file

addresses (see RA Rb register addresses in fig.3). It would have been obvious to one of ordinary skill in the art to use Yoshida in Moreno for including the subfield for specifying the register file address as claimed because the use of Yoshida could provide Moreno the capability to generate an access to a particular resource (e.g. register file or the like) based on a given request , and because Moreno did teach an operand field in his branch instruction for specifying a target address or destination address in a cache storage (see col.5, lines 49-59), which was a suggestion of the need for providing a temporally storage, such as a register file, or the like, to increase the access ability of the memory resource, for the above reason, provided a motivation.

31. As to claims 8-14, Moreno did not specifically show the format field as claimed . However, Yoshida taught a format filed (see fig.2 [FM], fig.22, col.6, lines 8-37). It would have been obvious to one of ordinary skill in the art to use Yoshida in Moreno for including the format field as claimed because the use of Yoshida could provide Moreno the ability to specify the instruction based on the format portion of the instruction, and because Moreno also taught that extra bits were used for predecoding the representation of the VLIW contents to simply execution, which was recognizable by one of ordinary skill in the art that predecoded extra bits were applicable for format representations in the instruction, such as the format instruction field, in order to provide additional information regarding the VLIW instructions.

32. As to claim 17, Yoshida also taught a threshold issue slot (see the 1st and 2nd and 3rd order to be issued in fig.2).

33. As to claim 18, Yoshida also taught the formatted instruction parameters such as the start [0], middle [92] , extension [x] and padding [94] (see fig.8 [0][92][96][]. As to the numbers of issue slots (see the issued operation filed in col.14, lines 12-24)).

34. Claims 19,20 are objected, for reciting the details of the encoded bits, to as being dependent upon a rejected base claim, but would be allowable, upon pending conditions of the "112", "101" and double patenting set forth in this action, if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

35. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Matsuzaki et al. (5,202,967) is cited for the teaching of the variable instruciton lenght format (col.3, lines 10-30) .

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

DANIEL H. PAN
PRIMARY EXAMINER
GROUP